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EXAMINER	
NGUYEN, LONG T	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 04/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/665,300	NAIR, RAJENDRAN	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-9 and 11-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-9 and 11-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/17/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the positive input of the first amplifier is coupled to the input signal through a first output level based buffer impedance modulator circuit and the positive input of the second amplifier is coupled to the input signal through a second output level based buffer impedance modulator circuit in claim 3.

Double Patenting

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1-4, 6-9, and 11-25 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-2 of U.S. Patent Number 6,717,445 (application 09/608,086),. Although the conflicting claims are not identical, they are not patentably distinct from each other because they recites substantially the same embodiment of the invention. Note that the renumbered claims 1-2 of U.S. Application 09/608,086 (which

will be public as U.S. Patent 6717445 on 4/6/04) recites a circuit which includes a signal input; a buffer circuit; a voltage following circuit; wherein the voltage following circuit includes a first; an NMOS transistor; a second amplifier; and a PMOS transistor; first and second impedance modulator circuits as recited in claims 1-4 of the instant application, and therefore also obvious to meets the method steps recited in claims 11-14, and the functions in claims 15-18. Note that it is an intended use to use the circuit as claims in claim 1 in any electronic system, and it is obvious that the circuit as claimed can be used in a signal distribution integrated system as a repeater circuit or buffer as recited in claims 6-9, or used in a microprocessor as recited in claims 19-22. Note, with respect to claims 22-25, although claims 1-2 of Patent 6,717,445 (application 09/608,086) recites a circuit rather than a machine-readable medium having stored thereon instruction, it is obvious to one having skill in the art to create a software representation from the given circuit for the purpose of modeling/simulation the circuit for design purposes and build from that model once done.

Specification

5. The disclosure is objected to because of the following informalities:

On line 14 of page 7, "a input" should be changed to --an input--.

Further, the specification fails to clearly describes a machine-readable medium having stored thereon instructions, which when executed by a set of processors, causes said set of processors to perform the steps in claims 22-25. Note that lines 7-12 of page 12 of the instant specification mentions a machine-readable medium, but does not clearly describe the set of processors execute the machine-readable medium causing the same set of processors to perform steps of claims 22-25. Appropriate correction is required.

Claim Objections

6. Claims 2, 4, 7, 20 and 21 are objected to because of the following informalities: Appropriate correction is required.

Claim 2, line 3, "a NMOS" should be changed to --an NMOS--.

Claim 4, line 2, "a NMOS" should be changed to --an NMOS--.

Claim 7, line 2, "a signal" should be changed to --the signal--.

Claim 20, line 3, "a NMOS" should be changed to --an NMOS--.

Claim 21, line 2, "a NMOS" should be changed to --an NMOS--.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 8, 13, 17 and 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 8, "a buffer circuit" on line 1 is unclear antecedent basis because it is not known whether it is the same as buffer circuit recited earlier (line 3, independent claim 1).

With respect to claims 13 and 17, the recitations "generating a high output signal substantially independent of power supply noise" and "for generating a low output signal substantially independent of power supply noise" are indefinite because they are misdescriptive. Note that, line 20 of page 6 of the instant specification only discloses that output signal 305 will be less depend on the power supply and more depend on the input signal301. Thus, the specification does not specifically disclose that it is independent of power supply noise.

With respect to claim 24, this claim is indefinite for the similar problems as discussed in claims 13 and 17.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1, 4, 5, 11-19 and 21-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Taylor (USP 5,644,255).

With respect to claims 1, 4, 6-9, 11, 15, 19, 21, and 22 the Taylor reference discloses processing system (Figure 1) comprising a circuit (202, Figure 4), wherein the circuit (202) includes: a signal input (input node of inverter 401) to receive a signal (VIN); a buffer circuit (401, 404, 403) to receive the input signal (VIN) and to generate a buffer circuit output (the junction of 403 and 404); and a voltage following circuit (203, 204) to receive the signal (VIN) and to generate a voltage following output (junction of transistors 403, 404, 203 and 204) wherein the buffer circuit output (the junction of transistors 403, 404, 203 and 204) and the voltage following circuit output are coupled to a circuit output node (node connected to VLINE). Note Figure 4 shows that the voltage following circuit (203, 204) includes an NMOS transistor (203) and a PMOS transistor (204). Note, because the structure of the circuit (202, Figure 4) is substantially same as applicant's invention (Figure 2), so it is reasonable to considered the circuit (202, Figure 4) as a repeater or buffer. Note, with claim 22, because the circuit is implemented, so it is inherent that disk or hard-drive that store the netlisted filed of the circuit which is used to

simulate the circuit when design is the machine-readable medium having stored thereon instruction.

With respect to claims 12, 16 and 23, it is seen in Figure 4 of the Taylor reference that the voltage following circuit (203, 204) includes means (203) for generating a logic high output signal when the input signal (VIN) is high because when the input signal (VIN) is high, transistor 203 is turned on to generate a logic high output (at the source of transistor 203); and means (204) for generating a logic low output signal when the input signal is low because when the input signal (VIN) is low, transistor 204 is turned on to generate a logic low output (at the source of transistor 204).

With respect to claims 13, 17 and 24, because the structure of the prior art (circuit 202 in Figure 4 of Taylor) is same to that of the claimed invention (Figure 2), the functions recited in these claims are considered to be inherent (MPEP 2112.01 and In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977)).

With respect to claims 14, 18 and 25, Figure 4 of the Taylor reference shows that the buffer circuit (401, 404, 403) includes a first inverter (401) including an input (input of 401) coupled to receive the signal (VIN) and an output (output of 401); and a second inverter (403, 404) including an input (the node connected gates of transistors 403 and 404) coupled to the output of the first inverter (401) and an output (junction of transistors 403, 404, 203 and 204) coupled to the circuit output node (node connected to VLINE).

Allowable Subject Matter

11. Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and if a proper terminal disclaimer is filed.

Claim 20 would be allowed because the prior art of record fails to disclose or suggest all the limitations of these claims. In particular, the prior art of record fails to disclose, in combination with other limitations, the voltage following circuit (706, 708, 702, and 704 in Figure 6) which includes a first amplifier (706, Figure 6), an NMOS transistor (702, Figure 6), a second amplifier (708, Figure 6) and a PMOS transistor (704, Figure 6) with the recited connection set forth in these claims.

Claim 3 would be allowed because it depends on claim 2.

12. Note that the scope of claims 2-3 is the same as claim 20, but cannot be indicated allowability at this time because, in rewritten claims 2 in an independent form, claims 2 and 3 may be rejected under 35 U.S.C. 101 because they would be duplicated of claims 1 and 2 of U.S. Patent 6,717,445.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 308-0956.

March 27, 2004

Long Nguyen
Art Unit: 2816